Amendment to the Claims:

Claims 1-24 (canceled)

25. (Currently Amended) A process for forming device isolation for a semiconductor assembly, said process comprising the steps of:

forming a first trench into a semiconductor substrate;

forming a single layer dielectric lining on the surface of said first trench;

forming a spacer along the sidewall of said first trench over and in direct contact with said single layer dielectric lining without removing a lateral portion of said single layer dielectric residing at the bottom of said first trench;

forming a second trench into said semiconductor substrate at the bottom of said first trench by removing said lateral portion of said single layer dielectric while ~~by~~ using said spacer as an etching guide;

forming an insulative material in said first and second trenches at least partially by substantially consuming said spacer and said single layer dielectric lining to substantially fill said first and second trenches with said insulative material without forming a diffusion region at the base of said second trench.

26. (Previously Amended) The process as recited in claim 25, wherein an overall depth of said first and second trenches is two times a depth of a bordering diffusion region.

27. (Original) The process as recited in claim 25, wherein said spacer is formed from an oxidizable material.

28. (Original) The process as recited in claim 25, wherein said spacer is formed of oxide.

29. (Original) The process as recited in claim 25, further comprising the step of forming an insulation layer on said semiconductor substrate prior to said step of forming a first trench.

30. (Previously Amended) The process as recited in claim 25, wherein said step of forming said insulative material comprises:

annealing said semiconductor assembly in the presence of an oxidizing agent.

31. (Previously Amended) The process as recited in claim 25, wherein said insulative material and said dielectric lining are the same type material.

32. (Withdrawn) The process as recited in claim 31, wherein said dielectric lining inhibits becoming oxidized.

33. (Original) The process as recited in claim 25, wherein said process uses only one mask to form said device isolation.

34. (Currently Amended) A process for forming device isolation for a semiconductor assembly, said process comprising the steps of:

forming a first trench into a semiconductor substrate;

forming a single layer dielectric lining on the surface of said first trench;
forming a semiconductive spacer along the sidewall of said first trench over and in direct contact with said single layer dielectric lining without removing a lateral portion of said single layer dielectric residing at the bottom of said first trench;

forming a second trench into said semiconductor substrate at the bottom of said first trench by removing said lateral portion of said single layer dielectric while ~~by~~ using said semiconductive spacer as an etching guide;

forming an insulative material in said first and second trenches at least partially by substantially consuming said semiconductive spacer and said single layer dielectric lining during formation to substantially fill said first and second trenches with said insulative material without forming a diffusion at the base of said second trench;

planarizing said insulative material;

wherein said process uses only one mask to form said device isolation.

35. (Previously Amended) The process as recited in claim 34, wherein an overall depth of said first and second trenches is two times a depth of a bordering diffusion region.

36. (Original) The process as recited in claim 34, further comprising the step of forming an insulation layer on said semiconductor substrate prior to said step of forming a first trench.

37. (Previously Amended) The process as recited in claim 34, wherein said step of forming said insulative material comprises:

annealing said semiconductor assembly in the presence of an oxidizing agent.

38. (Previously Amended) The process as recited in claim 34, wherein said insulative material and said single layer dielectric lining are the same type material.

39. (Withdrawn) The process as recited in claim 34, wherein said dielectric lining inhibits becoming oxidized.

40. (Currently Amended) A process for fabricating a semiconductor assembly having device isolation, said process comprising the steps of:

forming a mask over a silicon substrate assembly;

forming a first trench into said silicon substrate assembly using said mask as an etching guide;

forming an oxide layer on the surface of said first trench;

forming a silicon spacer on the sidewall of said first trench over and in direct contact with said single layer dielectric lining without removing a lateral portion of said single layer dielectric residing at the bottom of said first trench;

forming a second trench into said silicon substrate assembly at the bottom of said first trench by removing said lateral portion of said single layer dielectric while ~~by~~ using said silicon spacer as an etching guide;

forming an oxide filler in said first and second trenches at least partially by substantially consuming said silicon spacer and said oxide layer to substantially fill said first and second trenches with said oxide filler without forming a diffusion region at the base of said second trench;

planarizing said oxide filler.

41. (Previously Amended) The process as recited in claim 40, wherein an overall depth of said first and second trenches is two times a depth of a bordering diffusion region.

42. (Withdrawn) The process as recited in claim 40, further comprising the step of forming an insulation layer, comprising oxide and nitride, on said semiconductor substrate prior to said step of forming a first trench.

43. (Original) The process as recited in claim 40, wherein said step of forming an insulative material comprises:

annealing said semiconductor assembly in the presence of an oxidizing agent.

44. (Withdrawn) The process as recited in claim 40, further comprising the step of:

forming a conformal layer of polysilicon into said first and second trenches prior to said step of forming an oxide filler.

45. (Withdrawn) A process for fabricating a semiconductor assembly having device isolation, said process comprising the steps of:

forming a mask over a silicon substrate assembly;

forming a first trench into said silicon substrate assembly using said mask as an etching guide;

forming a nitride layer on the surface of said first trench;

forming a silicon spacer on the sidewall of said first trench;

forming a second trench into said silicon substrate assembly at the bottom of said first trench by using said silicon spacer as an etching guide;

forming an oxide filler in said first and second trenches, said oxide substantially consuming said silicon spacers and thereby substantially filling said first and second trenches;
planarizing said oxide filler.

46. (Withdrawn) The process as recited in claim 45, wherein an overall depth of said first and second trenches is two times the depth of a bordering diffusion region where the depth of the diffusion region is determined by the depth of an area containing at least approximately 90% concentration of conductive atoms.

47. (Withdrawn) The process as recited in claim 45, further comprising the step of forming an oxide layer on said semiconductor substrate prior to said step of forming a first trench.

48. (Withdrawn) The process as recited in claim 45, wherein said step of forming an insulative material comprises:

annealing said semiconductor assembly in the presence of an oxidizing agent.

49. (Withdrawn) The process as recited in claim 45, further comprising the step of:

forming a conformal layer of polysilicon into said first and second trenches prior to said step of forming an oxide filler.

50. (Currently Amended) A process for forming device isolation for a semiconductor assembly, said process comprising the steps of:

forming a trench into a semiconductor substrate having a top surface;

forming a single layer dielectric lining on the surface of said trench;

forming a semiconductive spacer along the sidewall of said trench over and in direct contact with said single layer dielectric lining;

forming an insulative material in said trench at least partially by substantially consuming said semiconductive spacer and said single layer dielectric lining to substantially fill said trench with said insulative material without forming a diffusion region at the base of said trench; and

planarizing said insulative material to approximately the same level as the top surface of said semiconductor substrate.

51. (Previously Amended) The process as recited in claim 50, wherein an overall depth of said trench is two times a depth of a bordering diffusion region.

52. (Original) The process as recited in claim 50, further comprising the step of forming an insulation layer on said semiconductor substrate prior to said step of forming a trench.

53. (Previously Amended) The process as recited in claim 50, wherein said step of forming an insulative material comprises:

annealing said semiconductor assembly in the presence of an oxidizing agent.

54. (Previously Amended) The process as recited in claim 50, wherein said insulative material and said dielectric lining are the same type material.

55. (Withdrawn) The process as recited in claim 50, wherein said dielectric lining inhibits becoming oxidized.

56. (Original) The process as recited in claim 50, wherein said process uses only one mask to form said device isolation.